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1 **MEMORY INTERLACE-CHECKING METHOD**

2 **BACKGROUND OF THE INVENTION**

3 1. Field of Invention

4 The present invention relates to a memory interlace-checking method, which is
5 a test method that can detect weakened memory. Through interlacing data accesses,
6 the method can more accurately find memory problems.

7 2. Related Art

8 Memory is an indispensable element in a computer system. It has a
9 deterministic influence on the stability of the system. As the capacity and speed of
10 the memory increase indefinitely, the current memory manufacturing technologies
11 reach a scale below 0.2 micrometers, a supply voltage below 3.3 volts, and an
12 operation speed over 133MHz. Under such a high density, a low operation voltage
13 and a high operation frequency, memory becomes very sensitive and is easily
14 damaged or weakened because of the manufacturing process, external signals or
15 noise generated inside, resulting in low stability. Therefore, how to accurately
16 quickly detect the memory weakening problem is an important subject studied by
17 test engineers.

18 According to the current state of the art in memory testing, there is a problem of
19 being unable to accurately detect memory weakening or instability. Usual memory
20 testing programs perform complicated state settings and data accesses through the
21 command pins, address pins, I/O pins of the memory to detect whether each
22 element in the memory is good or not. Taking data accessing as an example, if one
23 wants to check the continuity of a particular word line (W/L) in the memory, the
24 result can be obtained by employing a one-dimensional row access pattern to access

1 the particular W/L. If one wants to check the continuity of a particular bit line (B/L)
2 in the memory, the result can be obtained by employing a one-dimensional column
3 access pattern to access the particular B/L. In addition, A.J. van de Goor discloses
4 other methods such as a two-dimensional checkboard, the GALPAT, a sliding
5 diagonal scheme and a butterfly pattern in *Testing Semiconductor Memory* (John
6 Wiley & Sons, 1991) to provide better error detection effects.

7 Although conventional methods have many different memory testing styles,
8 the memory address accessing, however, is more or less the same. As shown in Fig.
9 6A, the matrix on the left-hand side of the drawing represents the memory. Each
10 little square refers to a memory cell. On the right-hand side is a simplified way of
11 showing the ordering of addresses. In Fig. 6A, continuous address accessing is
12 performed from left to right and then from top to bottom. Another method from
13 bottom to top is employed in Fig. 6B. Figs. 7A and 7B show the memory address
14 accessing performed from right to left and then from top to bottom and from
15 bottom to top, respectively. Figs. 8A and 8B show the memory address accessing
16 performed from top to bottom and then from left to right and from right to left,
17 respectively. Figs. 9A and 9B show the memory address accessing performed from
18 bottom to top and then from left to right and from right to left, respectively.
19 However, no matter what memory accessing scheme is taken, it is still a vertical or
20 horizontal continuous access style (read, write or refresh). This kind of one bit by
21 one bit access method cannot effectively detect memory weakening problems.
22 That is, as shown in Fig. 6A, when accessing the first row from left to right,
23 electromagnetic interference (EMI) may result in weakening in the next row.
24 However, after finishing the access of the first row and starting the access of the

1 second row, the second row may be strengthened from a weakened state to a normal
2 state due to write-in, read or refresh. Therefore, the foregoing continuous memory
3 address accessing scheme cannot effectively detect the memory weakening
4 problems. The conventional memory test methods are neither stringent nor
5 accurate and thus have to be improved.

6 SUMMARY OF THE INVENTION

7 One objective of the invention to provide a memory interlace-checking method,
8 which can accurately detect memory weakening problems.

9 Another objective of the invention to provide a memory interlace-checking
10 method, which is not only applicable to normal DRAM but also to the new
11 generation of DDR-DRAM and RDRAM.

12 Yet another objective of the invention to provide a memory interlace-checking
13 method consisting of a main step and a data checking step. The main step performs
14 command actions only on local memory (such as even rows or columns, or odd
15 rows or columns). The data checking step checks the portion in the memory that is
16 not triggered in the previous step so as to accurately determine whether the memory
17 has a weakening problem. This method can thus solve the problem of being unable
18 to stringently and accurately detect weakening problems in the conventional tests.

19 A further objective of the invention to provide a memory interlace-checking
20 method that has a main step and a data checking step. The memory addresses in the
21 main step and the data checking step are complementary to each other. In practice,
22 the memory address accessing can be performed from left to right, from right to left,
23 from top to bottom or from bottom to top.

24 The memory interlace-checking method in accordance with the present

1 invention includes: a main step having at least a main datum, which performs
2 command actions on the memory address row or column; a data checking step
3 having at least a data check datum, which checks memory rows or columns not
4 triggered in the main step; wherein by accessing particular memory rows or
5 columns, other yet to be triggered memory rows or columns may be weakened by
6 electromagnetic interference (EMI) and thus can be accurately detected in the data
7 checking step.

8 BRIEF DESCRIPTION OF THE DRAWINGS

9 Figs. 1A and 1B is a diagram of a first embodiment of the memory interlace-
10 checking method in accordance with the present invention using left to right
11 passes;

12 Figs. 2A and 2B is a diagram of a second embodiment of the memory
13 interlace-checking method in accordance with the present invention using right to
14 left passes;

15 Figs. 3A and 3B is a diagram of a third embodiment of the memory interlace-
16 checking method in accordance with the present invention using top to bottom
17 passes;

18 Figs. 4A and 4B is a diagram of a fourth embodiment of the memory
19 interlace-checking method in accordance with the present invention using bottom
20 to top passes;

21 Figs. 5 are diagrams of other possible embodiments of the memory interlace-
22 checking method in accordance with the present invention using passes in opposite
23 directions; and

24 Figs. 6A, 6B through 9A, 9B are schematic views of conventional memory

1 address accessing methods.

2 DETAILED DESCRIPTION OF THE INVENTION

3 The test method in accordance with the present invention can more accurately
4 detect memory weakening problems. This method is different from conventional
5 address accessing continuous sequential address accessing. The present invention
6 uses an interlacing data access technique. The method in accordance with the
7 present invention is composed of at least two steps: the main step and the data
8 checking step. In the main step, there are main data for executing commands. The
9 data perform the write, read, or refresh command in local addresses in the memory
10 (such as from left to right or from right to left in odd or even columns or rows).

11 While accessing the odd columns (rows), the yet to be accessed memory addresses,
12 *i.e.*, the even columns (rows), are weakened by the electromagnetic interference
13 (EMI) induced from the previously mentioned command actions. Afterwards, the
14 data checking step provides checking commands that checks addresses yet to be
15 triggered in the main step, *i.e.*, the even columns (rows). This can readily detect
16 weakened elements. So the present invention provides a method that can more
17 accurately determine whether memory is weakened.

18 The actual implementation of the present invention does not have extra
19 limitation as long as the memory accesses are interlacing. That is, there are many
20 different embodiments of the invention. The left hand side and central portion of
21 Fig. 1A show the memory access sequence and order in the main step 10 and the
22 data checking step 20, respectively, of a first embodiment of the memory
23 interlace-checking method. The arrow indicates the direction. "D" in the drawing
24 refers to the action location. The right hand side of the drawing shows a simplified

1 action sequence. Therefore, according to Fig. 1A, the main step 10 performs
2 command actions on the odd rows (1, 3, 5...) of the memory from left to right and
3 progressing from row to row in a top to bottom sequence. The command actions
4 include writing, reading and refreshing. Such actions will induce circuit actions
5 inside the memory and the resultant EMI. After the main step 10 is completed, the
6 data checking step 20 checks the memory rows that have not been accessed in the
7 main step, also from left to right and from top to bottom. These are the even rows
8 (2, 4, 6...) shown in the central portion of Fig. 1A. The main step and the data
9 checking step can also be understood from the simplified diagram on the right hand
10 side of Fig. 1A.

11 During the main step 10 in Fig. 1A, the odd rows of memory are triggered, and
12 the corresponding positions in the adjacent even rows will be affected by EMI.
13 Therefore, in performing the data checking step 20, the problem of memory
14 weakening will become apparent as the corresponding memory element is accessed.
15 The weakened memory elements can then be detected.

16 In a second embodiment of the memory interlace-checking method shown in
17 Fig. 1B, data access commands are first performed on the odd rows, and the data in
18 the even rows are read out to see if they are affected. The only difference from FIG.
19 1A is that the row to row sequence of accessing the memory is from bottom to top
20 rather than top to bottom as in the first embodiment. The same effects can be
21 achieved using the second embodiment.

22 Figs. 2A and 2B depict a method similar to the method depicted in Figs. 1A and
23 1B. The difference between the embodiment depicted in Fig. 2 the embodiment
24 depicted in Fig. 1 is the right-to-left memory access within each row.

1 The embodiments of the method depicted in Figs. 3A and 3B first access the
2 odd columns and check the even columns with individual memory locations in a
3 column sequentially accessed from top to bottom. The embodiments of the method
4 depicted in Figs. 4A and 4B are similar to the embodiments in Figs. 3A and 3B, but
5 differ in that individual accessing of memory locations within a column progresses
6 from bottom-to-top in Figs. 4A and 4B rather than top-to-bottom as in the
7 embodiments in Figs. 3A and 3B. Furthermore, various methods shown in Fig. 5
8 are also feasible schemes of the invention. Since the detection methods disclosed
9 herein only differ in the memory accessing schemes, the invention not only applies
10 to current DRAM but also to the new generation of DDR-DRAM and RDRAM.

11 In summary, the present invention provides a new memory check method that
12 is different from the continuous memory accessing in the prior art. Through the
13 division of memory into rows or columns, reading, writing, or refreshing command
14 actions are imposed on odd or even rows or columns, which induces signals and
15 EMI on the neighboring rows or columns yet to be accessed. Such
16 phenomena may weaken the already weak memory units so that these memory units
17 can be detected in the data checking step.

18 Certain variations would be apparent to those skilled in the art, which
19 variations are considered within the spirit and scope of the claimed invention.